

WHAT IS CLAIMED IS:

- 1 1. A programmable integrated circuit including a memory block, the
2 memory block comprising:
3 a plurality of address recycling multiplexers each having a first address input
4 coupled to receive address signals, and a select input coupled to receive an address stall
5 signal;
6 a plurality of address registers each having a data input coupled to an output of
7 a corresponding one of the address recycling multiplexers, and an output coupled to a second
8 input of the corresponding one of the address recycling multiplexers; and
9 an address decoder coupled to the outputs of the address registers.
- 1 2. The programmable integrated circuit of claim 1 wherein each of the
2 address registers has a clock input coupled to receive a clock signal.
- 1 3. The programmable integrated circuit of claim 2 wherein the memory
2 block further comprises:
3 a second plurality of multiplexers configurable to couple programmable
4 interconnect lines to the address recycling multiplexers.
- 1 4. The programmable integrated circuit of claim 1 wherein the memory
2 block further comprises:
3 an array of SRAM memory cells; and
4 data registers coupled to receive data signals and to transmit the data signals to
5 the array of memory cells.
- 1 5. The programmable integrated circuit of claim 1 wherein the
2 programmable integrated circuit is a field programmable gate array that is part of a system on
3 a chip.
- 1 6. A method for storing address signals during a stall state of a cache
2 memory, the method comprising:
3 providing address signals at first inputs of address recycling multiplexers;
4 coupling the first inputs of the address recycling multiplexers to data inputs of
5 address registers when an address stall signal is in a first state;
6 providing the address signals to an address decoder;

7 providing decoded address signals from the address decoder to the cache
8 memory; and
9 coupling output terminals of the address registers to second inputs of the
10 address recycling multiplexers when the address signal is in a second state during a refresh of
11 the cache memory.

1 7. The method of claim 6 wherein providing the address signals at the
2 first inputs of the address recycling multiplexers further comprises:
3 coupling interconnect lines to the first inputs of the address recycling
4 multiplexers through second multiplexers.

1 8. The method of claim 6 wherein providing the address signals to an
2 address decoder further comprises:
3 transmitting each set of the address signals from the data inputs to the output
4 terminals of the address registers in response to every other edge of a clock signal.

1 9. The method of claim 6 further comprising:
2 generating the address stall signal in a programmable logic block in response
3 to a refresh of the cache memory.

1 10. The method of claim 6 further comprising:
2 providing data to the cache memory using data registers.

1 11. The method of claim 6 wherein the address multiplexer, the address
2 registers, the address decoder and the cache memory all reside within a circuit block a
3 programmable integrated circuit.

1 12. The method according to claim 11 wherein the programmable
2 integrated circuit is part of a system on a chip.

1 13. A integrated circuit including a memory block, the memory block
2 comprising:
3 an address decoder circuit block;
4 address registers coupled to inputs of the address decoder circuit block and
5 coupled to receive a clock signal at clock inputs;

6 an address recycling block that causes the address registers to store address
7 signals during multiple cycles of the clock signal when an address stall signal is in a first
8 state,
9 wherein the address recycling block has first inputs coupled to receive the
10 address signals, second inputs coupled to outputs of the address registers, a select input
11 coupled to receive the address stall signal, and outputs coupled to data inputs of the address
12 registers.

1 14. The integrated circuit as defined in claim 13 wherein the address
2 recycling block includes a plurality of multiplexers coupled in parallel between the first and
3 second inputs and the outputs of the address recycling block.

1 15. The integrated circuit as defined in claim 13 wherein the address
2 signals are coupled to the first inputs of the address recycling block through programmable
3 multiplexers and driver circuits.

1 16. The integrated circuit as defined in claim 13 wherein the integrated
2 circuit is a field programmable gate array, and the address stall signal is generated by a
3 programmable logic block.

1 17. The integrated circuit as defined in claim 16 wherein field
2 programmable gate array is part of a system that includes a processor and a memory unit.

1 18. The integrated circuit as defined in claim 13 wherein the integrated
2 circuit operates the memory block as a cache memory.

1 19. The integrated circuit as defined in claim 13 wherein the memory
2 block includes an array of SRAM memory cells, and the address decoder circuit block selects
3 word lines in the SRAM array.